ChangXin Memory Technologies (688825 CH)

China's Rising DRAM Champion Amid The Memory Supercycle

Highlights

- As China's largest DRAM maker, CXMT is well-positioned to benefit from vast import substitution opportunities and a sustained peak DRAM cycle.
- We expect CXMT to achieve solid progress in HBM, with rapid capacity ramp-up and yield improvements boosting production in 2026-28. The extreme scarcity of HBM in China will help alleviate margin pressure from yield loss.
- Initiate coverage with BUY and a target price of Rmb59.40.

Analysis

- **Largest DRAM maker in China.** ChangXin Memory Technologies (CXMT) is China's dynamic random-access memory (DRAM) champion and ranks fourth globally in both revenue and bit shipments. We estimate that its market share in bit shipments will expand from 8.5% in 2025 to 10.7% in 2028, driven by rapid capacity expansion and improvements in yield.
- **DRAM supply bottleneck through 2026-28 sustaining elevated DRAM prices.** We expect global DRAM bit supply to grow at a three-year CAGR of 23.6% in 2026-28, while demand is forecasted to grow 28.7% during the same period. This will lead to a supply shortfall of 2.4%/13.5%/14.0% in 2026-28 respectively, which is projected to sustain elevated ASPs and margins going forward. We also expect an improved product mix from CXMT, with the proportion of high-value computer memory products such as double data rate (DDR) 5 and high-bandwidth memory (HBM) 3E in bit shipment rising from 31.9% in 2026 to 45.3% in 2028, supporting 336.2%/52.8%/4.3% yoy growth in blended ASP in 2026-28.
- **HBM will start to contribute more meaningfully in 2027-28.** We expect CXMT to start ramping up HBM production meaningfully from 2027 to address the severe shortages faced by Chinese players. We also expect production yield to improve from 20-30% currently to 30-40% by 2028. This, coupled with capacity expansion and solid pricing power, will bolster HBM contribution to revenue from under 1.0% in 2025 to 11.7% by 2028.
- **Capacity expansion outpacing peers.** Compared with global leading integrated device manufacturers' (IDM), CXMT's greenfield capacity takes 1-2 years of preparation, significantly shorter than overseas peers' 4-6 years. This flexibility allows CXMT to benefit from rapid expansion amid a supercycle. We expect CXMT's group capacity to grow at a three-year CAGR of 26.7% in 2026-28, adding 290,000 wafer starts per month to 12" wafer capacity by 2028 to fulfil robust demand from its domestic clients.
- **Initiate coverage with BUY and a target price of Rmb59.40 based on 11.2x 2027 EPS of Rmb5.30**. Our PE multiple is on a par with global DRAM IDMs' average upcycle valuation.

Key Financials

Year to 31 Dec (Rmbm)	2024	2025	2026F	2027F	2028F
Net turnover	24,178	61,799	390,048	675,094	934,674
EBITDA	10,383	35,859	359,699	609,119	835,912
Operating profit	(5,841)	8,773	325,815	561,022	760,206
Net profit (rep./act.)	(7,145)	1,875	169,659	360,012	506,024
Net profit (adj.)	(7,145)	1,875	169,659	360,012	506,024
EPS (fen)	(12)	3	250	530	745
PE (x)	n.a.	1,315.4	16.4	7.7	5.5
P/B (x)	57.1	43.5	9.6	4.4	2.5
EV/EBITDA (x)	273.3	79.7	7.1	3.6	2.2
Dividend yield (%)	0.0	0.0	0.0	0.0	0.0
Net margin (%)	(29.6)	3.0	43.5	53.3	54.1
Net debt/(cash) to equity (%)	54.3	50.3	(44.1)	(57.9)	(61.3)
Interest cover (x)	n.a.	2.9	71.8	126.9	181.5
ROE (%)	(8.4)	1.5	51.2	48.8	40.0
Consensus net profit	-	-	189,562	317,154	394,147
UOBKH/Consensus (x)	-	-	0.90	1.14	1.28

Source: CXMT, UOB Kay Hian

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BUY	
Share Price	Rmb40.97
Target Price	Rmb59.40
Upside	45.0%
Previous TP	n.a.

Stock Data

Sector	Semiconductors
Bloomberg ticker	688825 CH
Shares issued (m)	67,884
Market cap (Rmbm)	2,781,212
Market cap (US$m)	414,031
Avg daily t'over (US$m)	2,166

Price Performance (%)

High/low since listing				Rmb61.80 / Rmb38.11
1mth	**3mth**	**6mth**	**1yr**	**Since IPO**
(15.2)	(23.4)	n.a.	n.a.	373.1

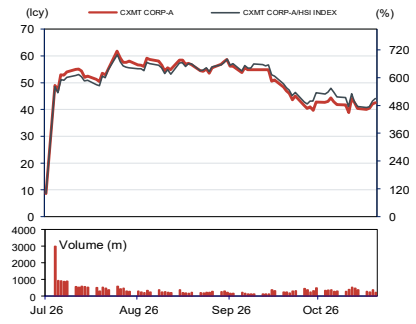
Major Shareholders (%)

Qinghui Jidian	19.21
Changxin Jicheng	10.38
National IC Fund II	7.74

Balance Sheet Metrics

2025 NAV/Share (Rmb)	7.43
2025 Net Debt/Share (Rmb)	(3.30)

Price Chart



Source: Bloomberg

Company Description

ChangXin Memory Technologies is China's largest DRAM manufacturer and the world's fourth largest by revenue. It designs and fabricates DDR4/DDR5, LPDDR4x/5/5x and LPDDR6 DRAM and memory modules at wafer fabs in Hefei and Beijing.

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Investment Highlights

- **Largest DRAM maker in China riding on DRAM supercycle.** CXMT is China's leading DRAM IDM and ranks fourth in the world by bit volume. We estimate CXMT's share of global DRAM bit shipments could grow from 8.5% in 2025 to 10.7% in 2028, driven by rapid capacity additions and improving yields. The strong underlying demand for DRAM is primarily underpinned by a broad surge in AI-related demand, as well as import substitution in the face of the US' tightening export restrictions on HBM. Apart from its strong position among domestic consumer electronics players, the company has secured orders from Chinese cloud service providers (CSP) for server-grade DDR5, and has broken into the supply chains of overseas brands including Apple, HP and Asus, thanks to their supply-source diversification incentives.

China's DRAM champion could see its share of global DRAM bit shipments rise from 8.5% in 2025 to 10.7% in 2028.

- **DRAM shortage likely to last through 2028…** Our global DRAM supply-demand forecast shows a sustained shortage in 2026-28, with the shortfall widening from a low single-digit percentage of supply in 2026 to a low-teens percentage in 2027-28. AI infrastructure is the primary driver, as demand from servers and GPUs lifts AI infrastructure's share of bit consumption to 60.0% in 2028, up 11.3ppt from that in 2025. On the other hand, while we expect AI adoption at the edge to lift DRAM consumption in PCs and smartphones, we remain cautious on their shipment numbers and are conservative on their content gains, as we expect most DRAM resources to go to higher-productivity products such as AI servers and GPUs. As a result, the share of DRAM bits consumed by PCs and smartphones could fall to 4.5%/30.3% in 2028 respectively, down 4.8ppt/5.7ppt from 2025.

Supply shortages every year in 2026-28; servers and GPUs are projected to consume 60.0%/62.9%/66.4% of total DRAM bits in 2028-30.

- **…and DRAM prices to remain elevated on product mix improvements.** The supply shortfall through 2028 leaves limited room for price moderation. While some commodity DRAM products may face a price ceiling, we anticipate ongoing opportunities for price hikes in AI-server DRAM products, which include HBM, DDR5 RDIMMs/MRDIMMs, and SOCAMM. Server-related products should also continue to take a larger share of bits, giving DRAM makers more room to optimise their product mix. As such, we foresee sustained growth, with CXMT's blended ASP per Gb rising 336.2%/52.8%/4.3% yoy in 2026-28.

AI-server DRAM products are leading the price hikes.

- **HBM adds second leg of growth from 2027-28.** We understand that CXMT began HBM3E risk production in Sep 26, with mass production planned for late-27. We expect CXMT to ramp up wafer allocation to HBM to 3.5%/12.5%/19.3% of total wafer starts in 2026-28, and production yield is also expected to improve by 10-20ppt from the early ramp-up phase now to about 30-40% by 2028. On top of that, we estimate that China will face an 87.5%/46.2%/28.8% HBM supply shortfall in 2026-28 if we only account for domestic production, and the severe supply shortage is likely to support more aggressive price hikes heading into 2027. Capacity expansion and yield improvements could drive HBM revenue expansion of 49.1x/3.6x yoy in 2027-28 to Rmb30.7b/Rmb109.3b respectively, with its contribution to total revenue surging to 4.5%/11.7%.

Chinese AI chip makers have stocked up HBM inventory for next few months but procurement is increasingly challenging.

- **Flexible capacity expansion a significant edge.** CXMT is known to to build greenfield fabs in 1-2 years, much faster than overseas competitors who need 4-6 years, mainly thanks to favourable government policies that expedite construction and resource-allocation priority that supports a round-the-clock build schedule. This flexibility lets CXMT capitalise on the supply shortage faster than its peers. We expect group capacity to grow at a three-year CAGR of 26.7% in 2026-28, adding 290,000 wafer starts per month (wpm) of 12-inch wafer capacity to reach 570,000 wpm in 2028. This will allow CXMT to outpace its rival majors, namely Samsung Electronics, SK Hynix and Micron Technology, as it is backed by a healthy operating cash flow and government-associated funds.

Capacity is growing at a three-year CAGR of 26.7% in 2026-28 to 570,000 wpm in 2028.

Valuation

- **Initiate coverage with BUY; target price: Rmb59.40.** Our target price is based on 11.2x 2027 PE based on EPS of Rmb5.30. Our PE multiple is on a par with global DRAM IDMs' average upcycle valuations. Note that the market is now pricing in a "late cycle" valuation for the DRAM industry (ie low single-digit PE multiples) as price hikes are slowing down. However, with the supply shortfall peaking in 2028, we expect revenue and margins to remain elevated through 2027-28, with earnings growth supported by AI-related demand, an improved product mix, resilient pricing, and capacity expansion. As such, we continue to price CXMT at an average upcycle valuation at this point.
- **Profit after tax as a more meaningful indicator of financial performance.** CXMT's profit attributable to shareholders is heavily impacted by minority interests. Two of its current subsidiaries, which control Hefei Fab 2 (and future expansion in Hefei) and the Beijing Fab, are close to 70%/60%-owned by the local governments and external parties while CXMT maintains a controlling share. We foresee rapid expansion at these two fabs, which will lead to a surge in their net profit contribution from 37.2% in 2026 to 59.8% by 2030, which means minority interest will also remain elevated in 2026-30.
- CXMT repurchased a stake of about 10% in Changxin Jidian – the holding company of the Beijing fab – in mid-26 and has raised its stake to 42% as of today. We expect CXMT to continue with such buybacks in both Changxin Xinqiao (Hefei Fab2) and the Beijing fab given the vast amount of cash being generated through the 2026-28 supercycle. That said, forecasting this impact is challenging because these buybacks are sporadic and hard to predict on an annual basis. As such, the market has been paying more attention to its PAT performance instead of net profit attributable to shareholders.
- For reference, if we use PAT per share (Rmb7.39) and the same 11.2x 2027 PE, our target price will surge to Rmb82.80.
- **Risks.** A sharper mid-cycle drop-off in AI compute demand leading to sharp deterioration in DRAM prices, further tightening of export controls limiting CXMT's access to critical inspection and backend tools, and execution of HBM production ramp-up and yield improvements.

Figure 1: Valuation – CXMT VS Global DRAM Majors

Company	Ticker	Jul 04 - Jun 06	Jul 09 - Jun 10	Oct 12 - Dec 14	Jul 16 - Oct 18	Jul 20 - May 22	All five upcycles	Current forward PE (x)
Micron Technology	MU US	33.0	7.5	7.9	4.5	16.2	13.1	4.7
Samsung Electronics	005930 KS	10.3	7.8	8.6	7.9	11.3	9.3	2.5
SK Hynix	000660 KS	5.2	7.0	6.7	4.4	16.3	7.5	2.6
Nanya Technology	2408 TT	14.4	n.m.	7.0	6.0	14.6	10.2	3.2
Winbond Electronics	2344 TT	39.6	15.7	17.3	12.0	9.0	15.9	2.6
Average of Micron, Samsung, SK Hynix		16.2	7.4	7.7	5.6	14.6	10.0	3.3
Average of all five		20.5	9.5	9.5	7.0	13.5	11.2	3.1

Source: Visible Alpha, respective companies, UOB Kay Hian

Business Outlook

- **The DRAM shortage is projected to last through 2030.** We expect a DRAM supply shortfall of 2.4% of supply in 2026, widening to 13.5%/14.0% in 2027-28. The supply of older products, particularly conventional low-power double data rate (LPDDR) 4x and DDR4, should start to ramp up in 2028, which may moderate their ASPs, while conventional LPDDR5/DDR5 prices should remain more resilient through the year. Greenfield memory fabs will start scaling up in 2028 and will contribute more meaningfully from 2029, which should improve the overall supply-demand landscape, with the global shortfall narrowing to 12.0%/8.5% in 2029-30 respectively.
- **AI infrastructure drives bit demand growth at a five-year CAGR of 25.7% in 2026-30.** Demand is driven primarily by DRAM content per device. We expect server shipments to grow moderately at a five-year CAGR of 12.0% in 2026-30, while DRAM content per accelerator expands from 128GB-288GB in current-generation products up to 1TB by 2030, lifting server bit demand at a five-year CAGR of 33.8%. This makes AI infrastructure the single largest end-market for DRAM by 2030, at 66.4% of global DRAM bit demand, up from 48.6% in 2025.

Top-of the-line AI accelerators are expected to consume 1TB of memory per unit by 2030. CPUs are also projected to see a jump in DRAM content and volume.

- **Conventional consumer devices: PCs and smartphones will consume more memory, but growth will be limited by supply.** OEMs of these consumer devices will struggle to absorb rising costs, which will tighten their supply in 2026-28. The supply-demand balance is likely to improve in 2029 as legacy players in mainland China, such as SwaySure Technology Co and Fujian Jinhua Integrated Circuit Co (JHICC), and in Taiwan, such as Nanya Technology Corporation, start to ramp up greenfield capacity, although the supply of high-end LPDDR5x and DDR5 should remain tight given the strong demand pull from AI infrastructure. That said, meaningful breakthroughs in on-device AI agents will be a major catalyst for PCs and smartphones: substantial productivity gains and value creation from on-device agents will markedly increase consumer willingness to accept price hikes. We have yet to factor this in fully given the limited visibility of such breakthroughs.

Automobiles and embodied robots may use a few hundred GB of DRAM per unit.

- **Physical and edge AI applications may add a new source of demand.** Next-generation physical AI applications, such as automotive and industrial, and intelligent edge devices will see a meaningful increase in the use of DRAM content to support smarter features, with examples being Level 3-4 advanced driver assistance systems (ADAS) in cars, wider deployment of embodied devices, and more on-device intelligence as AI and large language model (LLM) adoption expands. That said, we expect supply-side bottlenecks and the relatively slower pace of development to limit a meaningful acceleration in the next five years. As such, we expect automotive/industrial DRAM consumption to grow at a five-year CAGR of 24.2%/15.7% in 2026-30, and their share of bit demand will trend down 0.2ppt/0.7ppt to 3.8%/1.3% in 2030 as AI infrastructure-related demand outgrows the market.

With improved DRAM availability, PCs and smartphones will readily absorb more memory. For example, Apple's M7 Ultra is rumoured to utilise 1.5TB of unified memory.

Figure 2: DRAM Supply-Demand Balance Forecasts

(Exabytes, EB)	2026F	2027F	2028F	2029F	2030F
PC	3.4	3.1	3.5	4.0	4.2
Smartphone	16.7	21.2	23.5	26.2	28.3
Graphics and gaming	5.6	8.2	10.8	14.1	18.6
Automotive	1.9	2.4	3.0	3.6	4.4
Servers	20.5	28.3	35.8	45.3	57.2
Industrial and others	0.8	0.9	1.1	1.2	1.5
Bit demand (EB)	**48.9**	**64.1**	**77.6**	**94.4**	**114.2**
yoy (%)	*34.4*	*31.1*	*21.2*	*21.6*	*20.9*
Bit supply (EB)	**47.7**	**56.5**	**68.1**	**84.3**	**105.2**
yoy (%)	*32.2*	*18.3*	*20.6*	*23.8*	*24.8*
Supply less demand (EB)	**(1.2)**	**(7.6)**	**(9.5)**	**(10.1)**	**(9.0)**
Sufficiency, supply / demand - (%)	**(2.4)**	**(13.5)**	**(14.0)**	**(12.0)**	**(8.5)**

Source: UOB Kay Hian

- **CXMT's G5 node is reaching 1anm-1bnm equivalent bit density.** CXMT started migrating to its G4 platform (16nm, 1x-1znm) in 2H24, and by 1H26 almost all of its output was on G4 with production yields surpassing 90%. In Sep 26, CXMT announced the commencement of mass production on its G5 DRAM platform, which is also built on a 16nm node but with bit density raised by 50% to a level closer to the 1anm-1bnm node, according to CXMT's disclosure. We expect the production ramp-up, platform migration and yield improvements through 4Q26-2027 to lead to a maturity yield of 80-90% by mid-28, when CXMT is likely to start ramping up production of G6, a 12-13nm/1cnm-equivalent node. This will allow CXMT to upgrade its product mix further, raise bit output and improve power efficiency and thermal properties.

During node migration, CXMT has to take production lines offline for tool upgrades, which may affect utilisation, shipments and profitability.

Figure 3: Platform Upgrade Roadmap

(%) of wafer production	1Q24	2Q24	3Q24	4Q24	1Q25	2Q25	3Q25	4Q25	1Q26	2Q26	3Q26	4Q26	1Q27	2Q27	3Q27	4Q27	1Q28	2Q28	3Q28	4Q28
G2 (19nm)	65	52	37	17	6	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G3 (17nm)	35	48	57	64	58	52	32	18	7	2	-	-	-	-	-	-	-	-	-	-
G4 (16nm)	-	-	6	19	36	45	68	82	93	98	95	85	70	60	45	30	15	5	-	-
G5 (15-16nm)	-	-	-	-	-	-	-	-	-	-	5	15	30	40	55	70	85	95	95	90
G6 (12-13 nm)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	5	10

Source: CXMT, TrendForce, UOB Kay Hian

- **4F²: CXMT is circumventing the US technology blockade with a different scaling path.** CXMT announced in Oct 26 its plans to produce engineering products for a server-grade DDR5 registered dual in-line memory module (RDIMM) using a 4F² cell design by year-end. 4F² stands the access transistor vertically (Vertical-channel transistor (VCT)/Vertical surround gate (VSG)), which relaxes the lithography design rules by roughly 20% compared with 6F² at the same capacitor pitch. This allows CXMT to stay on deep ultraviolet (DUV) multi-patterning longer.

  However, it shifts the process burden to high-end wafer fab equipment (WFE) optimised for vertical structures: high-aspect-ratio (HAR) etchers for pillar/channel definition and verticality, selective oxide or silicon nitride (SiN) dielectric etch, atomic layer deposition (ALD) for conformal gate and capacitor dielectrics, and titanium nitride (TiN) or similar deposition tools. Hybrid bonding is also typically required to separate the array and periphery. Top-of-the-line inspection and metrology tools remain essential for controlling the tall, narrow features and bonding alignment.

  The switch to 4F² architecture may shrink cell area by about one-third versus 6F² at the same feature size, producing a further 30-50% bit density gain at the chip level once periphery overhead is included. As such, 4F² is now considered to be one of the optional routes for CXMT to scale beyond G6.

  However, there will be a steep learning curve in scaling and yield improvement for 4F² (Appendix IV). Much of the specialised WFE required – especially inspection and metrology tools, and certain HAR and selective-etch modules – still relies on foreign suppliers, which are subject to US export restrictions. Vertical-channel formation, hybrid bonding and increased process complexity also raise defect risks and lower initial yields. We also understand that CXMT's next-generation G6 node (ramp-up from 2028) will achieve a 30% die area shrinkage via a partial adoption of CXMT's 4F² vertical-channel architecture, which makes 4F² more of a multi-year technology/production ramp, intended to give CXMT a second scaling option alongside continued 6F² scaling instead of a singular technological route.

The 4F² server-grade DDR5 RDIMM is likely to use wafer-to-wafer hybrid bonding; back-end tools are not covered by US restrictions.

Figure 4: CXMT Expected To Remain 2-3 Years And Two Generations Behind The Three Major DRAM IDMs

	2026	2027	2028	2029	2030
CXMT	G4 / 1znm	G5 + 4F2? / 1anm-1bnm	G5 + 4F2? / 1anm-1bnm	G6 + 4F2? + 3D DRAM? / 1cnm	G6 + 4F2? + 3D DRAM? / 1cnm
Samsung	1cnm	1dnm	1dnm + 4F2?	0anm + 4F2?	0anm + 4F2?
SK Hynix	1cnm	1dnm	1dnm	1dnm + 0anm	0anm
Micron	1γnm (1cnm)	1δnm (1dnm)	1δnm (1dnm)	1ε (1enm)	1ζ (0anm)

Source: CXMT, TrendForce, UOB Kay Hian

- **Monolithic 3D DRAM is another major direction for CXMT.** In theory, monolithic 3D DRAM is fabricated via a process like that used for 3D NAND. However, as DRAM has much stricter requirements for thermals, uniformity, noise, and current leakage – alongside significantly larger layer sizes – fabricating 3D DRAM is far more complex, making mass production unlikely in the near future. That said, 3D DRAM is considered one of the preferred routes for CXMT to scale beyond G6. Thus, similar to $4F^2$, CXMT and domestic equipment supply chain players have been co-developing tools designed for 3D DRAM, with notable progress in the past few years. Our checks indicate that CXMT is planning to deploy 3D DRAM in risk production by late-28. This suggests that there is a chance that 3D DRAM, alongside $4F^2$, is being considered for use on a G7 or G8 platform. This is again a few years ahead of foreign peers' timeline, now pencilled in for 2030-32, but it is necessary for CXMT to keep scaling beyond the limits of DUV tools.

G6 is likely to stay on $6F^2$ while implementing some VCT/VSG aspects. Whether G7 will utilise 3D DRAM or $4F^2$ is more uncertain.

- **CXMT is expanding its capacity aggressively to capture the ongoing memory supercycle.** By end-26, CXMT will have three fabs in full production – Hefei Fab 1, Hefei Fab 2 and Beijing Fab 1 – with a total capacity of 300,000 wpm. We understand that CXMT plans to build at least three more fabs by 2030, namely Hefei Fab 3 from 2H27, Beijing Fab 2 from 1H28 and Hefei Fab 4 from 2H28, as well as an HBM and advanced-packaging fab in Shanghai. This could nearly double its capacity to 570,000 wpm by end-28, and lift it to 780,000 wpm by end-29 and 820,000 wpm by end-30 as the Shanghai fab expands to 220,000 wpm, exceeding Micron's capacity by then.

We assumed CXMT has clinched export licences for advanced WFE tools, but tightening export restrictions may put our assumptions at risk.

- **Flexible capacity expansion bolsters growth.** We understand that CXMT is expanding its capacity faster than its global peers. Overseas, a greenfield fab typically takes 4-6 years to go through the various phases of expansion: planning, which can take two years or more, shell construction (1-2 years), equipment qualification and installation (1 year), and then risk production (1 year). CXMT moves much faster, taking only 1-2 years, thanks to: a) strong government support, which provides fast-track land, construction and environmental approvals, easy financing and prioritised utility construction, cutting both the planning phase and cleanroom construction to about one year, against 2-4 years for foreign players; and b) strong ties to a highly flexible domestic supply chain, with shorter lead times and faster qualification. CXMT collaborates with domestic WFE suppliers to accelerate import substitution. According to our checks, CXMT's general import substitution rate is near 50%, and could accelerate further to 60% by 2028.

Figure 5: Global Memory Fab Wafer Starts By Company (year-end)

	2026F	2027F	2028F	2029F	2030F
Samsung ('000 wpm)	750	855	940	1,070	1,310
yoy (%)	15.4	14.0	9.9	13.8	22.4
SK Hynix ('000 wpm)	615	695	800	940	1,160
yoy (%)	12.8	13.0	15.1	17.5	23.4
Micron ('000 wpm)	385	440	580	695	745
yoy (%)	13.2	14.3	31.8	19.8	7.2
CXMT ('000 wpm)	300	400	570	780	820
yoy (%)	7.1	33.3	42.5	36.8	5.1
Global capacity ('000 wpm)	2,085	2,625	3,190	3,855	4,475
yoy (%)	13.6	25.9	21.5	20.8	16.1

Source: Respective companies, Trendforce, UOB Kay Hian

Figure 6: CXMT Share Of Industry Bit Supply

	2026F	2027F	2028F	2029F	2030F
Industry DRAM bit supply (b Gb)	382	452	545	675	842
yoy (%)	32.2	18.3	20.6	23.8	24.8
CXMT bit output (b Gb)	37.8	44.0	58.4	78.7	111.4
yoy (%)	53.2	16.5	32.7	34.6	41.6
CXMT share of industry bit supply (%)	9.9	9.7	10.7	11.7	13.2

Source: Respective companies, Trendforce, UOB Kay Hian

We expect a decline in CXMT's bit shipment market share in 2027 due to a higher allocation to low-yield HBM.

- **Bit share is increasing.** Thanks to fast-tracked capacity expansion, yield improvements and node migration, CXMT's bit output is expected to grow at a five-year CAGR of 35.2% in 2026-30, against 23.9% for the global supply, lifting its share of industry bit supply from 8.5% in 2025 to 13.2% in 2030. We believe CXMT is being held back by its capacity allocation to HBM, where its yield is estimated to be significantly lower than that of its foreign peers and of its own conventional DRAM, at only 20-30% currently, ie 30% frontend yield and 70% backend yield. As such, any meaningful breakthrough in its HBM progress would bring further upside.
- **CXMT is ramping up production of server-grade products.** CXMT has historically been mainly a conventional DRAM supplier focused on LPDDR products – LPDDR4 and LPDDR5 – used in consumer devices such as smartphones and PCs. However, CXMT officially launched in Nov 25 a 64GB DDR5 RDIMM, a server-grade product, and has since signed long-term agreements with Chinese CSPs and chip makers, including Alibaba, ByteDance and Huawei. With capacity growing rapidly and production yield at a mature mass-production level, we expect DDR5's share of total bit shipments to rise from 19.4% in 2025 to 47.8% in 2030, and its share of revenue from 31.6% in 2025 to 58.4% in 2028 and 57.0% in 2029, driving both sales growth and margin expansion. This matters as: a) server-grade DDR5 carries a higher ASP than LPDDR5x; and b) DDR5 pricing is likely to be far more resilient from 2028 onwards, given a tighter supply and higher exposure to AI-server and AI-infrastructure customers, who can absorb cost increases much more easily than consumer electronics makers.
- **HBM production yield curve could surpass market expectations.** We estimate that HBM contributes only around 0.2% of CXMT's bit shipments and revenue in 2026, due to a combination of low wafer allocation and low production yield. We expect CXMT to use W2W hybrid-bonding tools to start mass producing HBM3E 8H/12H in 2027, with 12.5% of wafer starts allocated to HBM. We understand that CXMT's HBM production yield may reach 25-30% in 2027, up from 20-30% currently for HBM3/3E, and it is likely to climb towards 40% by 2028. Besides improving production yield, CXMT will allocate more resources to HBM development and production, driven by vast domestic demand from local CSPs and AI-accelerator makers. We expect HBM's share of CXMT's bit shipments to expand to 4.8% by 2028 and 8.3% by 2030, and its revenue contribution to rise considerably to 11.7% by 2028 and 28.8% by 2030 due to its significantly higher ASP.
- **LPDDR: CXMT is shifting to LPDDR5x as it moves away from legacy products.** We estimate that LPDDR4x still contributes 36.3% of CXMT's bit shipments in 2026. However, as a legacy product, LPDDR4x is more exposed to oversupply and to the industry cycle, so we expect CXMT to shift capacity gradually to the more resilient LPDDR5x, DDR5 and HBM in 2027-29, and to exit LPDDR4x fully by 2030.

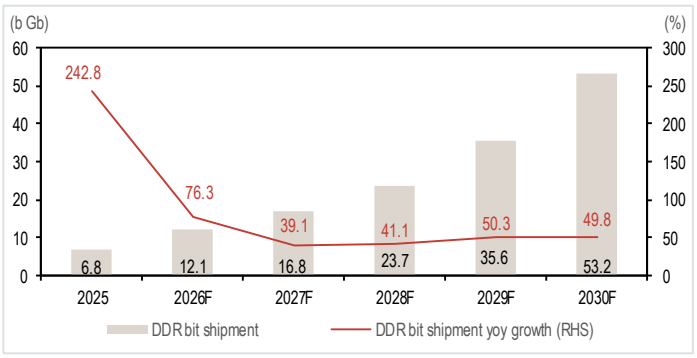
  In addition, CXMT launched its first LPDDR6 product in 3Q26, which is now used in Chinese flagship smartphones such as Xiaomi's 18 Fold. We estimate LPDDR6's ASP is about 15.8% higher than LPDDR5x's, mainly due to lower production yield, and hence higher costs, and a more complex fabrication process (ie at G5). We expect LPDDR bit shipments to grow at a five-year CAGR of 11.6% in 2026-30, meaningfully slower than DDR5 and HBM given the higher base and lower resource allocation. As a result, LPDDR's share of bit shipments could shrink from 80.2% in 2025 to 43.9% in 2030. We view this as a positive for CXMT, as the prices of consumer-electronics DRAM products are poised to moderate from early-28.

  With the establishment of its Shanghai fab, we also expect CXMT to start developing high-end server grade LPDDR products, although consumer electronics-related products are likely to remain a major contributor in the coming 1-2 years.

LPDDR5x SOCAMM modules are used in high-end CPUs, which are not under export restrictions now.

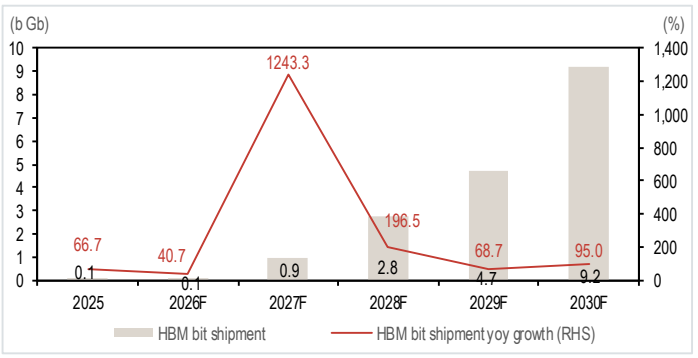
The Shanghai fab is set to focus on the development and production of high-end LPDDR, DDR and HBM products.

Figure 7: DDR Bit Shipment Forecasts



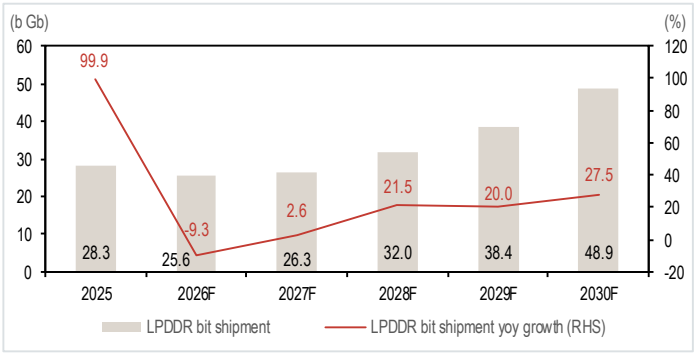
Source: CXMT, TrendForce, UOB Kay Hian

Figure 8: HBM Bit Shipment Assumptions



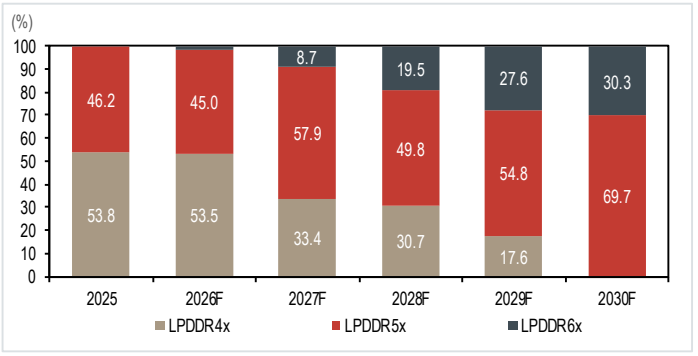
Source: CXMT, UOB Kay Hian

Figure 9: LPDDR Bit Shipment Forecasts



Source: CXMT, TrendForce, UOB Kay Hian

Figure 10: LPDDR Bit Mix By Generation

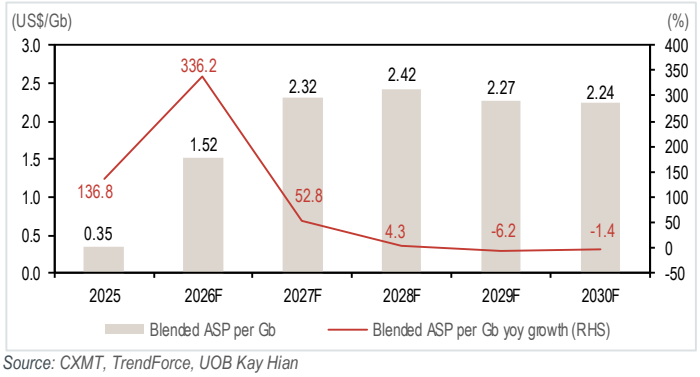


Source: CXMT, UOB Kay Hian

- **Blended ASP will remain on an uptrend through 2026-28.** Driven by supply shortages, quarterly price increases are projected to persist through 2026-27 across all product categories, driving a sharp 336.2%/52.8% rise in blended ASP per Gb in 2026-27. In 2028-29, we expect commodity DRAM prices to moderate as legacy capacity expansion by Chinese and Taiwanese players adds to conventional DRAM supply, slowing CXMT's blended ASP growth to 4.3% in 2028. That said, we expect shortages in server-related DRAM products (ie DDR5 RDIMM/MRDIMM, LPDDR5x SOCAMM and HBM) to persist, and the leading players to keep shifting capacity to these high-end products to protect their product mix and profitability. This should keep the commodity DRAM supply tight as well and cushion the price decline.
- **We expect CXMT to follow suit.** CXMT has launched a DDR5 RDIMM product and is expected to develop an LPDDR5x SOCAMM product going forward. We also expect its HBM yield to improve meaningfully to 35-50% by 2029-30. This richer product mix should keep CXMT's blended ASP 49.5%/47.5% above its 2026 level in 2029-30, even as commodity DRAM prices soften.

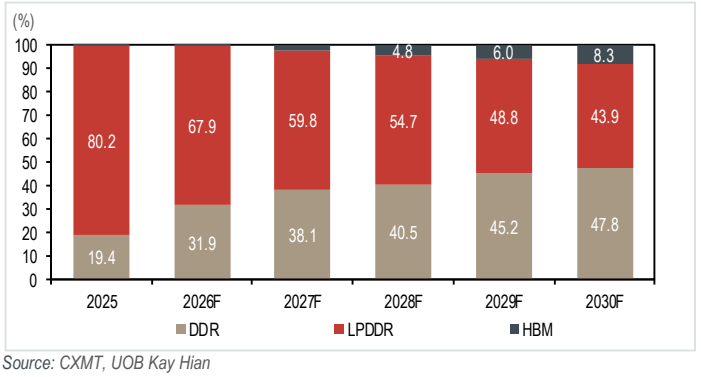
Commodity DRAM prices are close to the ceiling in 2027. As such, we adopt more conservative ASP assumptions in 2028.

Figure 11: Blended ASP Per Gb



Source: CXMT, TrendForce, UOB Kay Hian

Figure 12: DRAM Bit Mix By Product



Source: CXMT, UOB Kay Hian

Earnings Outlook

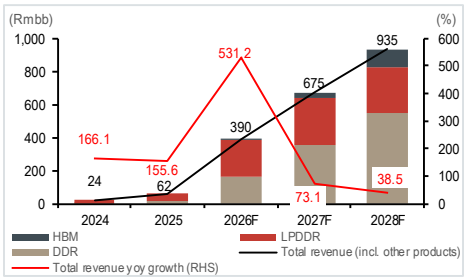
- **Revenue grows at a three-year CAGR of 147.3% in 2026-28.** We forecast revenue of Rmb390b/Rmb675b/Rmb935b in 2026-28 respectively, up 531.2%/73.1%/38.5% yoy. Of this, we expect DDR and LPDDR revenue to grow at a three-year CAGR of 203.5% and 89.7% in 2026-28 to Rmb546b and Rmb278b respectively in 2028. HBM revenue is projected to reach Rmb109b in 2028, or 11.7% of group revenue, as CXMT allocates more wafer resources to HBM to fulfil domestic HBM demand.
- **Gross margin stays above 80% in 2026-28.** We forecast gross margin of 87.7%/87.2%/85.3% in 2026-28 respectively, +46.7ppt/-0.5ppt/-1.8ppt yoy, with the 2027 decline driven by lower-yield, lower-margin HBM (38-61% gross margin in 2027-28) taking a larger share of the total mix. Opex ratio is expected to decline meaningfully from 26.8% in 2025 to 4.2%/4.0%/4.0% in 2026-28 respectively, primarily thanks to a better operating scale. This lifts EBIT margin from 14.2% in 2025 to 83.5%/83.1%/81.3% in 2026-28.
- **Net profit attributable to shareholders will be hit by a surge in minority interest, but profit after tax will register robust growth.** Given robust top-line growth, wide gross margins and a significantly improved operating scale, profit after tax is expected to grow at a robust three-year CAGR of 357.2% in 2026-28 to Rmb683b in 2028. However, profit attributable to shareholders will be impacted by sizeable minority interests – 41.0%/28.2%/25.9% of PAT in 2026-28 – from the rapid expansion of the partially-owned subsidiaries Xinqiao (Hefei Fabs 2-4) and Changxin Jidian (Beijing Fab). That said, we expect CXMT to buy back its stakes in both subsidiaries, thus net profit attributable to shareholders could rise 112.2%/40.6% yoy in 2027-28 to Rmb360b/Rmb506b respectively, against 74.5%/36.1% for profit after tax.
- **As operating cash flow funds the capex programme, CXMT moves into net cash.** We forecast capex of Rmb89b in 2026, up 79.3% yoy, rising 80.8%/65.6% yoy to Rmb161b/Rmb267b in 2027-28 respectively as the Xinqiao, Beijing and Shanghai fabs add capacity. We foresee accelerating capacity growth in 2027-28. We also expect CXMT to spend Rmb909m per 1,000 wpm of new capacity in 2026-30, much higher than the industry average of Rmb650m-700m, because we are assuming heightened WFE intensity as CXMT expands into more complex platforms and architecture.
- Operating cash flow covers 3.7x/3.4x/2.8x of capex in 2026-28 respectively, and we foresee free cash flow reaching Rmb238b/Rmb380b/Rmb480b. Net gearing moves from 50.3% as at end-25 to net cash of 44.1%/57.9%/61.3% of equity as at end-26/27/28 respectively.

Figure 13: Bit Mix, ASPs And Margins By Product

	2026F	2027F	2028F
LPDDR			
% of bits shipment	67.9	59.8	54.7
ASP	1.30	1.64	1.32
DDR			
% of bits shipment	31.9	38.1	40.5
ASP	1.98	3.24	3.50
HBM			
% of bits shipment	0.2	2.1	4.8
ASP	1.31	4.92	5.91
DDR Margin (%)	90.8	92.4	92.1
HBM Margin (%)	loss	38.2	60.8

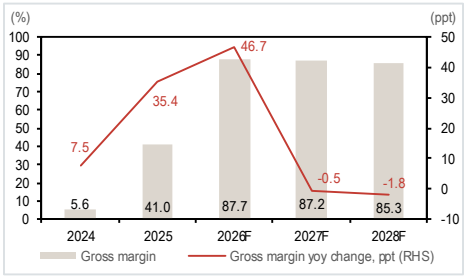
Source: UOB Kay Hian

Figure 14: Revenue Growth Breakdown



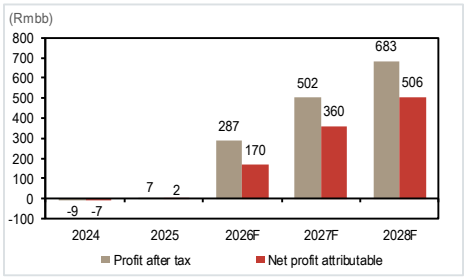
Source: CXMT, UOB Kay Hian

Figure 15: Gross Margin



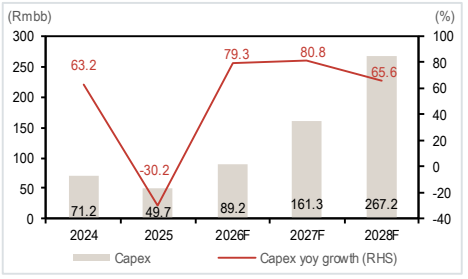
Source: CXMT, UOB Kay Hian

Figure 16: Profit After Tax And Net Profit Attributable



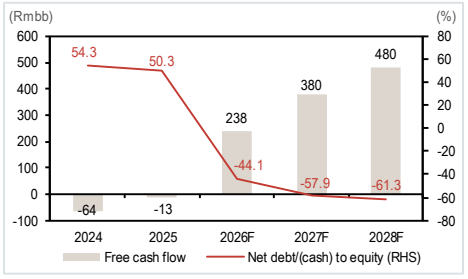
Source: CXMT, UOB Kay Hian

Figure 17: Capex



Source: CXMT, UOB Kay Hian

Figure 18: Free Cash Flow And Net Gearing



Source: CXMT, UOB Kay Hian

Profit & Loss

Year to 31 Dec (Rmbm)	2025	2026F	2027F	2028F
Revenue, net	61,799	390,048	675,094	934,674
Operating expenses	(53,027)	(64,233)	(114,072)	(174,469)
EBIT	8,773	325,815	561,022	760,206
Net interest income/(expense)	(2,954)	(3,913)	(171)	3,995
Other income/(expense)	1,882	(2,498)	(3,375)	(5,608)
Pre-tax profit	7,701	319,404	557,475	758,592
Tax	(557)	(31,940)	(55,748)	(75,859)
Minorities	(5,269)	(117,804)	(141,716)	(176,709)
Net profit (rep./act.)	1,875	169,659	360,012	506,024
Net profit (adj.)	1,875	169,659	360,012	506,024

Balance Sheet

Year to 31 Dec (Rmbm)	2025	2026F	2027F	2028F
Fixed assets	214,814	269,906	383,279	575,305
Other LT assets	10,985	11,209	11,031	10,451
Cash/ST investment	72,629	374,766	702,594	1,095,783
Other current assets	38,357	50,763	84,252	124,519
Total assets	336,785	706,645	1,181,155	1,806,058
ST debt	27,644	34,948	34,250	33,622
Other current liabilities	25,199	39,945	64,462	97,478
LT debt	119,801	112,821	106,538	100,885
Other LT liabilities	10,042	10,042	10,042	10,042
Shareholders' equity	56,754	289,557	634,625	1,112,410
Minority interest	97,346	219,332	331,238	451,621
Total liabilities & equity	336,785	706,645	1,181,155	1,806,058

Cash Flow

Year to 31 Dec (Rmbm)	2025	2026F	2027F	2028F
Operating	36,520	327,602	541,023	747,193
Pre-tax profit	7,701	319,404	557,475	758,592
Tax	3,957	(31,940)	(55,748)	(75,859)
Deprec. & amort.	27,086	33,884	48,096	75,706
Working capital changes	(7,579)	2,341	(8,972)	(7,251)
Non-cash items/others	5,354	3,913	171	(3,995)
Investing	(86,823)	(88,577)	(157,041)	(258,968)
Capex (growth)	(49,739)	(89,201)	(161,291)	(267,152)
Others	(37,084)	624	4,250	8,183
Financing	46,121	63,113	(56,155)	(95,036)
Dividend payments	-	-	-	-
Issue of shares	31,795	66,317	-	-
Proceeds from borrowings	75,507	10,000	10,000	10,000
Loan repayment	(60,230)	(9,676)	(16,980)	(16,282)
Others/interest paid	(951)	(3,528)	(49,175)	(88,754)
Net cash inflow (outflow)	(4,182)	302,138	327,828	393,189
Beginning cash & equivalent	42,508	37,798	339,935	667,763
Changes due to forex impact	(528)	-	-	-
Ending cash & equivalent	37,798	339,935	667,763	1,060,952

Key Metrics

Year to 31 Dec (%)	2025	2026F	2027F	2028F
Profitability				
Gross margin	41.0	87.7	87.2	85.3
EBITDA margin	58.0	92.2	90.2	89.4
Pre-tax margin	12.5	81.9	82.6	81.2
Net margin	3.0	43.5	53.3	54.1
ROA	0.6	32.5	38.1	33.9
ROE	1.5	51.2	48.8	40.0
Growth				
Turnover	155.6	531.2	73.1	38.5
EBITDA	245.4	903.1	69.3	37.2
Pre-tax profit	178.9	3,923.7	74.5	36.1
Net profit	n.m.	8,949.2	112.2	40.6
EPS	n.m.	7,923.9	112.2	40.6
Leverage				
Debt to total capital	45.7	20.3	11.3	6.9
Debt to equity	84.0	25.5	12.7	7.5
Net debt/(cash) to equity	50.3	(44.1)	(57.9)	(61.3)
Interest cover (x)	2.9	71.8	126.9	181.5

Appendix I – Company Background

- Established in 2016, CXMT is a leading Chinese integrated memory manufacturer specialising in the design, research and development, production and sale of DRAM chips. Since its inception, CXMT has established itself as a key participant in China's semiconductor ecosystem, supported by its impressive technical expertise, strong innovation capabilities and expanding portfolio of commercially available DRAM products.
- Headquartered in Hefei, Anhui, CXMT operates research centres and branches in China and overseas. The company offers a broad portfolio of DRAM products, including DDR5, DDR4, LPDDR5/5x and LPDDR4x chips and memory modules. These products are used across mobile devices, PCs, servers, virtual-reality equipment and Internet-of-Things applications. With integrated capabilities spanning chip design, R&D, manufacturing and sales, CXMT is able to address the diverse memory requirements of consumer, enterprise and emerging technology markets.
- Listed on the Shanghai Stock Exchange's STAR Market under stock code 688825 CH on 27 Jul 26, CXMT priced its offering at Rmb8.66 per share, equivalent to 309x diluted 2025 PE against an industry average of 76x. CXMT has expanded significantly in recent years through continued investment in R&D, manufacturing capacity and product development. The company's technological advancement and expanding product portfolio position it as an important contributor to China's semiconductor self-sufficiency and an emerging competitor in the global DRAM market.

Milestones

Year	Events
2016	Established and initiated the first phase of its Hefei DRAM manufacturing base.
2017	Commenced construction of the first phase of its Hefei DRAM manufacturing base in March.
2018	Completed construction of the first-phase Hefei fabrication facility and began equipment installation in January. Completed validation tape-out and trial production of 8Gb DDR4 engineering samples in July.
2019	Showcased its 8Gb DDR4 product at the World Manufacturing Conference in September. Received its first commercial order and officially launched product sales in November.
2020	Initiated the first phase of its Beijing DRAM manufacturing project in June.
2021	Commenced the second phase of its Beijing DRAM manufacturing project in December.
2022	Began operating the trial production line for the first phase of its Beijing DRAM project in January. Completed structural construction of the main fabrication facility for the second phase of its Hefei DRAM project in June.
2023	Completed its conversion into a joint-stock company. Launched its LPDDR5 product series, including 12Gb dies and 6GB and 12GB packaged memory products.
2024	Commenced mass production of DDR5 products, marking its expansion into a new generation of mainstream PC and server memory chips. Completed a Rmb10.8b equity financing round involving state-owned, financial and strategic investors.
2025	Commenced mass production of 8,533Mbps and 9,600Mbps LPDDR5x products and began customer sampling of its 10,667Mbps product. Showcased its DDR5 and LPDDR5x product portfolios at IC China.
2026	Listed on the Shanghai Stock Exchange's STAR Market under stock code 688825 CH on 27 July. Raised approximately Rmb57.9b through its IPO, representing the largest mainland Chinese semiconductor offering at the time.

Source: CXMT, UOB Kay Hian

Management Profile

Name	Age	Position	Experience
Zhu Yiming	54	Chairman	Chairman of the company since Feb 21. MSc. Previously served as a senior engineer at iPolicy Networks Inc and project manager at Monolithic System Technologies Inc. Founded GigaDevice in 2005 and served as its General Manager from Apr 05 to Jul 18; has remained Chairman of GigaDevice since Apr 05. Served successively as Director, Chairman and CEO of CXMT from Jul 18 to Apr 23, and as the company's CEO from May 20 to Apr 23.
Cao Kanyu	55	Director; President; Core Technical Personnel	Director since Jun 21; has served successively as CEO and President since Apr 23. PhD. Worked at Philips Semiconductors in the US and Hyperband Communications from May 02 to Jun 05. Founded Beijing Kuntian Ke Microelectronics and Beijing Fandaxun Technology between Jul 05 and Aug 13, and led NovoMem Inc's NAND flash business from Nov 13 to Oct 17. Joined CXMT in Nov 17 and subsequently held senior R&D, product and general management roles, including Executive Vice President of Ruili Integrated Circuit, Executive Vice President of Product R&D and Technology R&D at CXMT, and General Manager of ChangXin Jidian.
Zheng Rui	44	Director; Audit Committee Member	Director of the company since May 25. Serving as Party Branch Secretary, Executive Director and General Manager of the company since Oct 24. PhD. Held investment, risk-control and management positions at Anhui Provincial Investment Group and its affiliates from Jul 10. Served as Deputy General Manager of Anhui Wan Investment Asset Management from Jul 17 to Oct 24, and as Party Branch Secretary from Dec 21.
Fang Wei	57	Director	Director of the company since Aug 22; Chief Economist of the group since Feb 22. College diploma; Senior Accountant. Worked at the former Hefei Fertiliser Plant, Hefei Sifang Chemical Group and Hefei Industrial Investment Holding, among other organisations, from Aug 91 to Jan 22. Served as General Manager of the Planning and Finance Department of Hefei Industry Investment Holding (Group) from Mar 15 to Jan 22.
Wei Jun	59	Director	Director of the company since Jun 23. MSc. Served in planning and development functions of China's machinery-electronics and information-industry authorities from Jul 90 to Mar 08. Deputy Director-General of the Planning Department of the Ministry of Industry and Information Technology from Mar 08 to Jul 15. Vice President of China Integrated Circuit Industry Investment Fund since Jul 15.
Hou Huawei	46	Director	Director of the company since Aug 25. MSc. Began his career as a ship-market analyst at China State Shipbuilding Corporation's industry research centre in Jul 01. Worked at China Development Bank from May 06 to Oct 11 and again from Aug 13 to Apr 23, holding senior appraisal and industry-review roles. Served as Deputy Director of Beijing Xicheng District's Financial Street Subdistrict Office from Oct 11 to Aug 13. Director and Vice President of Sino IC Capital since Apr 23.
Xie Shumin	54	Employee Director	Employee Director since Aug 25. BSc. Worked at Anhui Zhongwan Materials and Minerals, Anhui Keli Information Industry, the Hefei Economic and Technological Development Area Administrative Committee and China Fortune Land Development's Hefei business from Sep 94 to Apr 21. Joined CXMT in Apr 21 as Director of General Administration. Serving as a company director-level manager and trade-union head of the Party and Mass Affairs Centre since Oct 22. Served as Employee Supervisor and Chairman of the Supervisory Board from Jun 23 to Jun 25.
Chen Wuchao	56	Independent Director; Audit Committee Chair	Independent Director of the company since Sep 21. PhD. Project Manager at Zhonghua Certified Public Accountants from Aug 95 to Oct 98. Has taught at Tsinghua University since Oct 98 successively as Lecturer and Associate Professor. Independent Director of CNPC Capital since Jun 23 and CITIC Trust since Sep 23.
Li Hua	49	Independent Director; Audit Committee Member	Independent Director of the company since Jun 23. MSc. Worked at Sinopec International, Beijing Qiankun Law Firm and Tsinghua Holdings from Jul 97 to Jan 07. Partner at Beijing Tianyin Law Firm from Jan 07 to Jun 09 and Assistant General Manager of Beijing Jingyi Group from Jul 09 to Jun 11. Served as Senior Partner and Head of Capital Markets at Yingke Law Firm from Jul 11 to Jun 19; has been a senior/global partner at DeHeng Law Offices since Jun 19. Also holds independent directorships at Taiji Computer and Beijing Yusys Technologies.
Cai Yimao	48	Independent Director	Independent Director of the company since Jun 23. PhD. Senior Researcher at Samsung Electronics in Korea from Aug 06 to Aug 09. Served successively as Associate Professor, Professor and Department Head in Peking University's Department of Micro/Nanoelectronics from Aug 09 to Jun 21. Professor and Dean of Peking University's School of Integrated Circuits since Jul 21. Independent Director of Founder Technology since Apr 23 and Beijing Huazhuo Jingke Technology since Apr 25.
Guo Wei	44	Independent Director	Independent Director of the company since Jun 25. PhD. Assistant Professor at The Hong Kong Polytechnic University from Aug 12 to May 20. Associate Professor at China Europe International Business School since Jun 20. Independent Director of USI Electronics since Apr 23.
Zhao Lun	73	General Manager	General Manager since Oct 22. BSc. Worked at the former Ministry of Posts and Telecommunications' Semiconductor Research Institute, the IC Design Centre of the former China Academy of Telecommunications Technology and Datang Telecom's microelectronics branch from Feb 82 to Apr 02. Served as General Manager and Vice Chairman of Datang Microelectronics from Apr 02 to Feb 12, while also serving as a Director and Deputy General Manager of Datang Telecom. Later held senior roles at AVIC (Chongqing) Microelectronics and Beijing Chuang'an Microchip. General Manager and Executive Director of CXMT from Nov 17 to Oct 22. Company Director from Jun 23 to Aug 25.
Zhang Yu	56	Co-President	Joined the company in Sep 24 and currently serves as Co-President. MSc. Engineer at Aviation Industry Ministry Research Institute No. 606 and later Deputy General Manager of Beijing Ancor Communications from Jul 91 to Sep 02. Worked at BOE Technology Group from Mar 04 to Sep 24, serving successively as Director, Senior Vice President and Executive Vice President.
Zhu Wenju	59	Executive Vice President	Executive Vice President since Apr 25. MSc. Worked at Intel (China), NMX Philippines and other companies from Jul 93 to Jun 11. Served as General Manager and Vice President across Micron Semiconductor's Xi'an, Singapore and Malaysia operations from Jul 11 to Dec 21. Joined the company in Dec 21 and has held Senior Vice President and Executive Vice President roles.
Huang Danyang	58	Senior Vice President; Chief Financial Officer	Senior Vice President and Chief Financial Officer since Sep 22. PhD; ACCA member and Senior Accountant. Held finance roles at Nanjing Tianyue Group, United Biscuits China, Nanjing Pepsi and A. O. Smith China from Jul 91 to Jul 07. Served as Finance Director at Johnson Controls China Investment, Magna Automotive Technology (Shanghai), Shanghai Jizhi Information Technology and Whirlpool China from Jul 07 to Oct 18. Held Senior Director, Vice President and Senior Vice President roles at CXMT from Oct 18 to Sep 22.

Name	Age	Position	Experience
Feng Pengxi	52	Senior Vice President; Head of Strategic Investment	Joined the company in Aug 24; currently Senior Vice President. PhD; Senior Accountant and Senior Economist; formerly held CFA and FRM credentials. Worked in banking, treasury, financial management and corporate investment roles at ICBC, Huagong Tech, Yangtze Communications and Bank of China from Oct 96 to Feb 10. From 2010-20, served as Deputy General Manager and Chief Economist of Wuhan Financial Holdings and Chairman of Hubei Integrated Circuit Industry Investment Fund, and also served as Deputy Head of Wuhan's Jianghan District. From 2020 to Aug 24, held investment leadership roles at Xiaomi and Zhuhai Taihe Private Equity.
Yuan Yuan	45	Vice President; Board Secretary	Vice President and Board Secretary since Jun 23. BSc. R&D Engineer and Project Manager at Midea Group from Jul 04 to Nov 08. Served in section-head and department-head roles at BOE Technology Group from Nov 08 to Aug 18. Joined the company in Sep 18 and subsequently served as Director-level Manager, Senior Director and Vice President.
Li Hongwen	51	Senior Vice President; Core Technical Personnel	Has served successively as company's Vice President and Senior Vice President since Feb 23. BSc. Worked at the China Aeronautical Computing Technique Research Institute, Beijing Gaohong Xintong Technology and Beijing Changxun Xintong Technology from Sep 98 to Mar 03. Design Department Manager at Micron Semiconductor (Shanghai) from Mar 03 to Feb 17. Joined the company in Mar 17 and subsequently served as Design Director and Vice President of CXMT.
Tan Teck Hong (Chen Dehong)	46	Vice President, Fab Operations; Core Technical Personnel	Joined the company in Jun 22 and currently serves as Vice President of Fab Operations. MSc; Singapore citizen with Chinese permanent residency. Worked at Micron Technology, Inc in Singapore from Jul 05 to Apr 22.
Wang Dan	43	R&D Director; Core Technical Personnel	Joined the company in Jan 19 and currently serves as R&D Director. PhD; Chinese national with Korean permanent residency. Senior Engineer at Samsung Electronics in Korea from Sep 10 to Mar 18.
Tang Yanzhe	49	Technical Director; Core Technical Personnel	Joined the company in Nov 20 and currently serves as Technical Director. PhD. Worked at TPV Semiconductor (Shanghai), GlobalFoundries, the Institute of Microelectronics at A*STAR and NXP Semiconductors from May 04 to Nov 18. Served as Director at Green Silicon Storage Technology from Dec 18 to Nov 20.

Source: CXMT, UOB Kay Hian

Shareholder Structure

Shareholder	Shares (m)	Pre-IPO (%)	Post-IPO before over allotment (%)	Post-IPO after full allotment (%)	Lock-up
Hefei Qinghui Power Gathering Enterprise Management Partnership Enterprise (Limited Partnership)	13,043.8	21.67	19.50	19.21	36 months
Hefei ChangXin Integrated Circuit Co Ltd	7,047.8	11.71	10.54	10.38	36 months
China Integrated Circuit Industry Investment Fund Phase II Co Ltd	5,256.1	8.73	7.86	7.74	36 months
Hefei Jixin Enterprise Management Partnership (LP)	5,037.4	8.37	7.53	7.42	36 months
Anhui Provincial Investment Group Holding Co Ltd	4,760.5	7.91	7.12	7.01	36 months
Zhejiang Alibaba Cloud Computing Co Ltd	2,319.2	3.85	3.47	3.42	Later of 12 months from listing / 36 months from share acquisition
Hefei Chantou No.1 Equity Investment Partnership (LP)	1,111.1	1.85	1.66	1.64	36 months
GigaDevice Semiconductor Inc	1,085.7	1.80	1.62	1.60	12 months
Shenzhen Zhaoyin Yunting Growth Equity Investment Fund Partnership (LP)	952.1	1.58	1.42	1.40	12 months
Beijing Fengyi Enterprise Management Consulting Partnership (LP)	901.3	1.50	1.35	1.33	12 months
Hefei Jianchang Equity Investment Partnership (Limited Partnership)	901.3	1.50	1.35	1.33	12 months
Hexie Health Insurance Co., Ltd.	901.3	1.50	1.35	1.33	12 months
Top 10 shareholders (including ties)	**43,317.55**	**71.97**	**64.77**	**63.81**	

Source: CXMT, UOB Kay Hian

Appendix II – Risk Factors

EXPORT CONTROLS AND ACCESS TO ADVANCED WFE

Timeline Of US Memory And Semiconductor Restrictions Relevant To CXMT

Date	Actor	Measure	Who/what affected	Remarks / impact
Oct 18	US (BIS)	Fujian Jinhua Integrated Circuit Co (JHICC) added to the Entity List	Fujian Jinhua; DRAM	Direct Chinese-memory precedent: Entity List status imposed licensing requirements on all items subject to the US' Export Administration Regulations, with a presumption of denial. CXMT is not listed.
2018-19	US / Netherlands	US pressure on Dutch EUV licensing; no EUV shipment to China	ASML EUV lithography systems	ASML states that it has never shipped an EUV system to China. For CXMT, EUV is therefore unavailable as a production scaling route, increasing reliance on DUV-based patterning.
Nov 18	US (DoJ)	Criminal indictment over Micron trade secrets	Fujian Jinhua; UMC	Shows that trade-secret and IP enforcement is a separate risk channel from export licensing. This was a JHICC/UMC case, not a restriction on CXMT.
May 20	US (BIS)	Huawei's foreign-produced direct product rule expanded	Foreign-produced semiconductors made with specific US technology/ equipment for Huawei	Established a more extraterritorial semiconductor-control mechanism. The 2020 rule targeted Huawei, not CXMT, but became an important template for later semiconductor controls.
Dec 20	US (BIS)	SMIC and related entities added to the Entity List	SMIC and related entities	Company-specific precedent for a major Chinese fab: Entity List status materially tightened access to US-origin items. The action did not apply to CXMT.
Aug 22	US government	Licence requirement imposed on advanced Nvidia AI GPUs to China	Nvidia A100 and H100; related systems	Restricted access to leading US AI accelerators. This changes the demand environment for China's AI compute and memory, but is not a direct manufacturing restriction on CXMT.
Oct 22	US (BIS)	Advanced-computing and semiconductor-manufacturing controls	DRAM at <=18nm half-pitch; NAND >=128 layers; logic <=16/14nm	Most directly relevant US manufacturing control: The US' Bureau of Industry and Security, explicitly brought DRAM at <=18nm half-pitch within the advanced-node regime, increasing licensing risk for relevant tools, technology and US-person support.
Dec 22	US (BIS)	36 entities added to the Entity List, including YMTC	YMTC and other Chinese entities	Memory-sector precedent: YMTC was added to the Entity List while CXMT was not. The two Chinese memory suppliers therefore face materially different company-specific licensing regimes.
Jul 23	Japan (METI)	23 categories of advanced SME added to export control	Advanced semiconductor manufacturing equipment	Japan added 23 categories of advanced SME to export control. The measure applies globally; equipment exports to China covered by the measure generally require individual licensing.
Sep 23	Netherlands	National authorisation requirement for specific advanced SME	Specific advanced semiconductor manufacturing equipment, including advanced DUV	Introduced Dutch licensing for specific advanced semiconductor manufacturing equipment. For CXMT, key exposure is access to advanced immersion DUV; authorisations are on a case-by-case basis, not a blanket ban.
Oct 23	US (BIS)	Oct 22 controls updated and tightened	Advanced chips and semiconductor manufacturing equipment	Tightened and clarified the Oct 22 framework while retaining the 18nm DRAM threshold. The change raised compliance risk without changing the core DRAM cutoff.
Jan 24	Netherlands / ASML	Partial revocation of 2023 DUV shipment licences	ASML NXT:2050i and NXT:2100i systems	ASML confirmed partial revocation of shipment licences for NXT:2050i/2100i systems to a small number of China customers. Relevant to CXMT as a tool-availability risk; affected customers were not disclosed.
Sep 24	Netherlands	Dutch national authorisation requirement expanded	Additional advanced DUV semiconductor manufacturing equipment	Expanded Dutch licensing to more advanced DUV equipment. Applications remain on a case-by-case basis, so the measure tightens access without constituting a blanket export ban.
Dec 24	US (BIS)	HBM controls added; 24 SME types controlled; 140 Entity List additions	HBM, advanced SME and 140 PRC entities; CXMT not among the additions	Adds a separate product-level constraint on HBM and broadens advanced-SME controls. CXMT was not among the 140 Entity List additions, but any future HBM product must be assessed under the applicable HBM control parameters.
Jan 25	Netherlands	More national controls effective 1 Apr 25	Selected metrology and inspection technologies	Added selected metrology/inspection technologies to Dutch national licensing from 1 Apr 25, widening the controlled WFE set relevant to advanced process control.
Jul 25	US administration	H20 licensing policy reversed toward approved China sales	Nvidia H20	US policy shifted from an April halt toward licensed H20 sales to approved China customers. This is a demand-side change for China's AI players, not a relaxation of CXMT's manufacturing-tool controls.
Aug 25	US administration	15% US revenue-share arrangement linked to certain China AI-chip sales	Nvidia H20; AMD MI308	May increase licensed AI-chip availability in China, but does not change the semiconductor manufacturing equipment restrictions faced by Chinese fabs.
Jan 26	US (BIS)	H200, MI325X and similar chips moved to case-by-case licensing	Specific advanced AI accelerators	Changes AI chip availability under defined security conditions; does not directly relax CXMT access to advanced semiconductor manufacturing equipment.
Jun 26	US administration	Addition of CXMT and over 100 Chinese firms to the Entity List is put on hold.	CXMT and other Chinese firms	Key binary policy risk: Reuters reported CXMT had been approved for Entity List addition by an interagency committee but publication was held back. CXMT remains unlisted as of this report's date, but the risk is unresolved.
Jun 26	US (DoD)	CXMT included on the Section 1260H Chinese Military Companies list	CXMT	Separate from the Entity List: the designation does not itself impose Export Administration Regulations' export controls or broad sanctions, but it raises federal contracting and supply-chain compliance risk.

Source: BIS, respective companies, UOB Kay Hian

- **Export controls will be a major risk for CXMT going forward.** The Oct 22 US rule explicitly targets advanced DRAM manufacturing at <=18nm half-pitch, while Dutch and Japanese measures add licensing requirements across advanced lithography and other WFE. CXMT is not on the Entity List as of this report's date, but is still subject to country-wide export controls which restrict advanced WFE required for leading nodes. For example, the etch/deposition WFEs used in advanced nodes require licensing with a presumption of denial; and certain tools, such as ion-implantation and inspection/metrology, are strictly restricted if it is stated that they are intended for advanced memory. As such, access to advanced WFE remains one of the biggest risk factors for CXMT's expansion plans going forward, especially with ion-implantation and inspection/metrology tools where domestic development is slow. The lack of access to advanced WFE may bring downside risks to our expansion plan assumptions, particularly on new architectures like 4F2, 3D DRAM, and also HBM.
- **Backend tools might become a key focus.** With Chinese fabs (both logic and memory) becoming increasingly more reliant on advanced backend processes to keep up with global competitors, backend tools may be targeted for export controls. This is especially important for TSV, thinning tools and hybrid bonders as overseas players like Disco Corporation, BE Semiconductor Industries, and Tokyo Electron/Ebara Corporation still produce the best-in-class tools/components for these processes.

ASSESSING RISKS OF SLOWDOWN IN AIDC BUILDOUT

- **Another major concern in the market is a potential slowdown in AIDC buildout.** Current concerns mostly stem from supply bottlenecks in AIDC power shells. The concerns are driven by a combination of power shortages, grid connections, government official permits, local community pushbacks, etc, primarily coming from the US which is expected to contribute to 74.2%/65.0% of global ex-China AIDC buildout in 2027-28. Unease over the AIDC buildout has been mounting steadily in the past few months. However, market sentiment has further deteriorated significantly in November after the US' mid-term elections, with many governors voicing their support for tightening regulations and even pausing permit approvals after achieving victory in their respective states, including Texas which accounts for around 29% of the US' 2028 net additions. **This has led to concerns of delivery slippage of AIDC from 2028-29, and even project cancellations in the worst-case scenario which may lead to an oversupply of AI compute, which is generally bearish for a cyclical product like DRAM.**
- In order to determine the potential impact of AIDC delays, we conducted a sensitivity analysis based on information disclosed by SemiAnalysis – a well-known third-party semiconductor research house.
- First, we see minimal risk of a DRAM supply surplus in 2027. Most of the projects in all affected US states are already under construction, which means a reasonable base-case impact assumption should be around a -5% impact on the global AIDC buildout. In the worst case possible, if projects under construction without full permits are hit by the upcoming regulatory changes, the impact on the global buildout will be higher at 16.9%. However, if we consider the global DRAM supply shortfall, a 16.9% lower server DRAM consumption will still result in a 2.5% shortfall in the global DRAM supply.
- For 2028, the impact will be more meaningful. We calculated that a total AIDC buildout of 28.3GW will be subject to regulatory changes when the newly-elected governors take office in 2027, but only 19.2GW of those will be at risk of a meaningful pause and slippage going into 2029. In the worst-case scenario, all 19.2GW of high-risk AIDC additions will be delayed until 2029, which is equivalent to an estimated 18.2% of global AIDC additions if we cross reference SemiAnalysis' numbers. An 18.2% lower AIDC DRAM consumption will result in a slight DRAM supply shortage of 1.55%, according to our DRAM supply-demand assumptions for 2028.

Sensitivity Analysis Of US AIDC Buildout's Impact To DRAM Market

(GW)	2026	2027	2028
US net additions	18.1	38.0	62.2
Ex-US net additions ex-China	6.9	13.2	33.5
China AI DC additions	6.0	8.0	10.0
Global ex-China	**25.0**	**51.2**	**95.7**
Global incl. China	**31.0**	**59.2**	**105.7**
US share of global ex-China (%)	72.4	74.2	65.0
2027	**Bull**	**Base**	**Bear**
GW slipping out of 2027	2.0	3.0	10.0
% of US 2027 additions (if all US)	5.3	7.9	26.3
% of global ex-China 2027	3.9	5.9	19.5
% of global incl. China 2027	3.4	5.1	16.9
2028	**Bull**	**Base**	**Bear**
GW slipping out of 2028 (to 2029+)	**3.9**	**10.8**	**19.2**
% of US 2028 additions	6.2	17.3	30.9
% of global ex-China 2028 (95.7 GW)	4.0	11.2	20.1
% of global incl. China 2028 (China 10 GW)	3.6	10.2	18.2
(EB)	**2026F**	**2027F**	**2028F**
Server + graphics	26.04	36.49	46.55
Others	22.85	27.59	31.09
Base demand	48.89	64.08	77.64
Base case	n.a.	62.21	72.89
Bear case	n.a.	57.91	69.17
Total supply	47.73	56.48	68.11
Base case shortfall %	n.a.	(10.16)	(7.02)
Bear case shortfall %	n.a.	(2.53)	(1.55)
No-delay shortfall %	(2.42)	(13.45)	(13.99)

Source: SemiAnalysis, UOB Kay Hian

- **As such, even in the worst-case scenario, our sensitivity analysis indicates that the global DRAM supply will remain tight.** Moreover, the extremely bearish outcome is highly unlikely to materialise, as: a) AIDC remains one of the most important drivers of US economic growth for the foreseeable future, and governors are unlikely to impose policies that will significantly impair their states' economic activities; b) most of the permit halts will likely last for six months until Jul 27 with Texas potentially pausing for 8-9 months, and new approvals will likely restart through 2H27, which implies only a portion of the affected capacity will be delayed; c) we have yet to factor in any actions from DRAM suppliers as they can pause capacity ramp of new fabs; d) during the planning stage, AIDC developers usually have multiple sites to consider for every project before making the final decision on where to build, ensuring flexibility in case some of the sites are impacted by delays; and e) customers may place orders anyway given that the supply shortage is expected to last through 2030 and the AIDC buildout is only delayed and not cancelled.
- **The bottom line is that we see limited oversupply risk for the DRAM market despite overwhelming market concerns.**

Appendix III – Minority Interest Assumptions

Minority Interest Assumptions By Subsidiary

(Rmbm unless otherwise stated)	2026F	2027F	2028F	2029F	2030F
Hefei Fab 1 (Changxin Storage): CXMT stake (%)	100.0	100.0	100.0	100.0	100.0
net profit (Rmbm)	117,611	217,511	216,423	146,414	163,817
minority interest (Rmbm)	-	-	-	-	-
share of group profit after tax (%)	40.9	43.4	31.7	17.5	13.9
share of net profit attributable (%)	69.3	60.4	42.8	23.3	16.5
Hefei Fabs 2-4 (Changxin Xinqiao): CXMT stake (%)	30.7	40.7	50.7	60.7	70.7
net profit (Rmbm)	115,256	130,717	224,884	354,952	416,531
minority interest (Rmbm)	(79,895)	(77,541)	(110,913)	(139,567)	(122,127)
share of group profit after tax (%)	40.1	26.1	32.9	42.5	35.4
share of net profit attributable (%)	20.8	14.8	22.5	34.3	29.7
Beijing (Changxin Jidian): CXMT stake (%)	42.3	52.3	62.3	72.3	82.3
net profit (Rmbm)	65,665	134,453	174,389	240,814	362,231
minority interest (Rmbm)	(37,909)	(64,174)	(65,797)	(66,778)	(64,224)
share of group profit after tax (%)	22.8	26.8	25.5	28.8	30.8
share of net profit attributable (%)	16.4	19.5	21.5	27.7	30.1
Shanghai Fab: CXMT stake (%)	100.0	100.0	100.0	100.0	100.0
net profit (Rmbm)	(50)	35,196	84,604	112,205	263,680
minority interest (Rmbm)	-	-	-	-	-
share of group profit after tax (%)	(0.0)	7.0	12.4	13.4	22.4
share of net profit attributable (%)	(0.0)	9.8	16.7	17.9	26.6
Parent and consolidation: share of group profit after tax (%)	(3.8)	(3.2)	(2.6)	(2.4)	(2.5)
share of net profit attributable (%)	(6.5)	(4.5)	(3.5)	(3.1)	(3.0)
Group profit after tax (Rmbm)	287,463	501,728	682,733	834,712	1,176,501
minority interest (Rmbm)	(117,804)	(141,716)	(176,709)	(206,345)	(186,350)
minority interest / profit after tax (%)	41.0	28.2	25.9	24.7	15.8
Net profit attributable (Rmbm)	169,659	360,012	506,024	628,367	990,150

Source: CXMT, UOB Kay Hian

- The bulk of CXMT's new capacity coming online in 2026-30 will be owned by subsidiaries in which CXMT has minority (but controlling) stakes. For example, Changxin Xinqiao (Hefei Fab 2, and presumably Fabs 3-4) is now 30.68%-owned by CXMT, and Changxin Jidian (Beijing Fab) was 31.72%-owned before a 10.55% stake repurchase boosted that to around 42.27%. And while it is not publicly disclosed, we assume the Shanghai fab will be wholly owned by CXMT. Note that most of the new capacity coming online will be under these minority-owned subsidiaries, and as such minority interests will rise sharply in 2026-28.
- As seen in the table on the next page, we expect: a) partially-owned fabs to see bit output as a % of total shipment surge from 53.5-60.4% in 2025-27 to 62.2-72.2% in 2028-30; and b) their earnings contribution to expand meaningfully from 37.2% in 2026 to 59.8% by 2030.
- This structure helps share CXMT's capacity expansion costs (with the rest of the stake owned by state-owned or provincial government-owned funds). This was because CXMT – a late entrant in the DRAM industry – was incurring losses during the pre-supercycle era. With significantly improved earnings visibility and cash generation through 2026-28, such profit (loss) sharing structure is no longer required, and we expect CXMT to continue buying back its stake at the subsidiary level going forward in order to reduce the risks related to minority interests.
- Given stake buybacks' sporadic nature, we believe the market is now mainly looking at profit after tax to determine CXMT's actual financial performance. Our estimates have stake repurchases baked in, but if we assume no further changes going forward, we see our estimates of net profit attributable to shareholders declining 7.4%/15.7%/28.2%/31.2% in 2027-30 respectively. For a more detailed breakdown, please see the table on the next page.

Sensitivity – No Further Stake Buy-in At Partially-owned Subsidiaries

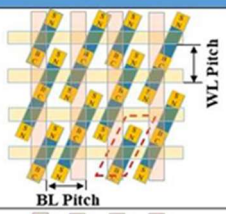
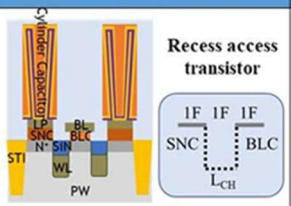
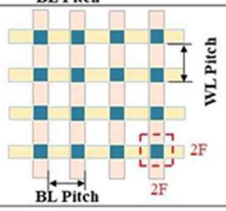
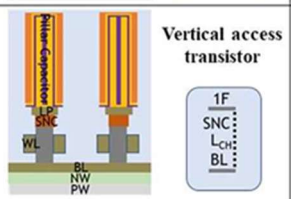
(Rmbm unless stated)	2026F	2027F	2028F	2029F	2030F
Xinqiao: CXMT stake (%)					
base case	30.7	40.7	50.7	60.7	70.7
no buy-in	30.7	30.7	30.7	30.7	30.7
Beijing: CXMT stake (%)					
base case	42.3	52.3	62.3	72.3	82.3
no buy-in	42.3	42.3	42.3	42.3	42.3
Net profit attributable (Rmbm)					
base case	169,659	360,012	506,024	628,367	990,150
no buy-in	169,659	333,495	426,653	451,039	681,623
change (%)	0.0	(7.4)	(15.7)	(28.2)	(31.2)
Cash required for stake buy-ins, base case (Rmbm; at the 2026 Beijing deal price of 1.5x book)					
Xinqiao	-	25,890	45,515	79,278	132,568
Beijing	9,500	18,863	39,049	65,231	101,385
Total	9,500	44,754	84,565	144,509	233,954
Cumulative	9,500	54,254	138,818	283,328	517,281

Source: CXMT, UOB Kay Hian

Appendix IV – 4F² Technology

- 4F² refers to the area of a DRAM cell. F is the unit the industry uses for the smallest feature size, and F² (F x F) is the unit used to measure the size of an individual cell. 4F² therefore means the cell occupies four units of F². This compares with the mainstream 6F² cell, which occupies six units of F², so in layman's terms, 4F² fits roughly 50% more cells into the same area, a meaningful boost over 6F².

A 6F² Cell Measures 3F x 2F, While A 4F² Cell Measures 2F x 2F

ITEMS	Layout	Profile map	Comments
6F² DRAM			Pros: ✓ Matured technology ✓ No floating body effect Cons: ✓ Lower bit-cell density ✓ Row hammer effect ✓ Short channel effect ✓ Process more complicated
4F² DRAM			Pros: ✓ Easier AA & NC patterns ✓ No BLC patterning ✓ higher bit density Cons: ✓ Difficult BL process ✓ Floating body effect

Source: CXMT

How is 4F² achieved?

- As seen in the figure above, a DRAM cell is made up of a transistor and a capacitor. In 6F² DRAM cells, the access transistor is formed in a recessed trench in the silicon, with its word line buried in the trench. The isolation and bit line contacts sit alongside it, and the cylinder capacitor sits on top of the access transistor. As the transistor is laid out horizontally, it takes up more surface area on the wafer.
- In 4F² cells, the transistor is formed as a vertical silicon pillar. The word line (WL, or gate) wraps around the pillar, ie gate-all-around (GAA), and the bit line is buried at the bottom of the pillars. Because this GAA VCT is built upwards rather than laid out horizontally as in 6F², it takes up less wafer area, which is what enables a higher density than conventional horizontal-channel transistors.
- VCT 4F² shares several fabrication processes with 3D NAND, such as: a) deep etch and conformal deposition, b) a gate wrapped around a vertical channel, and c) bonding of the periphery wafer onto the array wafer. As such, it is the preferred DRAM fabrication technology of NAND specialist Yangtze Memory Technologies Co (YMTC). We understand that the Chinese government has been facilitating technology sharing between memory companies (including YMTC and CXMT) in order to ease China's memory shortage. Thus, YMTC has ventured into the DRAM market, while CXMT's President announced that its first 4F² product, a DDR5 RDIMM, is due by end-26.
- That said, we believe 4F² is more of an optional route for CXMT, as the company is expected to begin the commercial production ramp of its G6 node with 6F² in mid- to end-28, while risk production of the next-generation 3D DRAM is slated to start in 2028-30. In contrast, YMTC is reportedly treating VCT 4F² as its core DRAM platform.
- CXMT will continue to use DUV as its core lithography tool. Fabricating GAA VCT also requires other advanced WFE, such as HAR etchers designed for vertical silicon pillar formation, oxide/SiN dielectric etch for WL isolation, ALD for the thin gate oxide, and TiN deposition for the gate. While domestic WFE suppliers are working closely with CXMT to develop these tools, we believe

foreign suppliers still provide much of this equipment, especially for inspection and metrology. A key question going forward is therefore how quickly CXMT can scale 4F² to mass production.

- VCT 4F² is seen as a stepping stone towards 3D DRAM which stacks many layers of cells on top of each other, similar to 3D NAND. Each layer has a horizontal transistor and a capacitor lying on its side, and the bit lines run vertically through the stack. Density comes from adding layers rather than shrinking features, so the process looks like that of NAND. It starts from an Si/SiGe superlattice grown by epitaxy, followed by a staircase, one deep etch through the whole stack, and the selective SiGe etch that hollows out each layer. Again, several core processes can be carried over from VCT 4F² to 3D DRAM.

Recent Chinese WFE Launches And Results For 4F² And 3D DRAM

Company	Product / result	What was disclosed	Application
AMEC	Primo Domingo	Gas-phase selective SiGe etch, >700:1 SiGe/Si in the lab; first unit shipped 22 Oct 26 to a domestic customer for validation	3D DRAM
AMEC	ICP etch (new generation)	140:1 aspect ratio with profile control in a 3D DRAM application; shipped to a leading domestic memory customer for qualification (1Q26 report)	3D DRAM
AMEC	Primo XD-RIE	70:1 to 90:1 aspect ratio, low-temperature etch, multi-level pulsed RF; launched at CSEAC 2026; a next-generation 90:1 low-temperature etcher was at a customer for validation by 1Q26	3D NAND, DRAM
AMEC	Prefima Unicore AM	12-inch ALD molybdenum tool, four reaction stations, for word-line fill in tall 3D stacks; launched at CSEAC 2026	3D NAND
NAURA	CSTIC 2026 paper	Two-step cyclic fluorine etch of Si/SiGe multilayers: >500:1 SiGe:Si, <10 Å Si loss per pass, >95% uniformity across 64-layer pairs	3D DRAM
NAURA	Acquisition of Nuohe Jianwei	Hybrid-bonding business bought for Rmb405m on 15 Oct 26	4F² VCT, 3D DRAM
Piotech	Dione 300 eX / Dione 300F eX / Pleione / Propus	Wafer-to-wafer hybrid bonding (at validation), fusion bonding, die-to-wafer bonding, pre-bond surface treatment	4F² VCT, 3D DRAM

Source: Respective companies, UOB Kay Hian

a) **Placing periphery circuitry on a separate wafer, followed by hybrid-bonding.** Both flows build the memory array on one wafer and the control circuits on another, then bond them together. This carries over completely: bonding, chemical mechanical planarisation (CMP) before bonding, and thinning are the same steps. This is the most direct equipment read-across for Piotech Inc's bonders and NAURA Technology Group Co's acquired bonding units.

b) **Gate-all-around transistor.** In VCT 4F², the word line wraps around a thin vertical silicon pillar, using ALD gate oxide, ISSG and ALD TiN. In 3D DRAM, once the SiGe is etched out, each remaining silicon layer becomes a thin horizontal channel, and the word line wraps around it again. The orientation changes, but the gate stack, the ALD tools and the know-how on leakage in a very thin channel carry over. CXMT's published research already describes its pillar as "more like a nanosheet".

c) **Capacitor materials.** The high-k dielectric deposited by ALD and the TiN electrodes stay the same. The geometry does not: VCT's capacitor stands vertically on top of the pillar, while in 3D DRAM it lies on its side inside the stack.

- Nevertheless, 3D DRAM seems to be still a few years away from mass production, and there is very limited information outside of R&D papers. The final production process utilised by CXMT can end up being very different compared with our current understanding.

Critical Process Steps For 4F²

Process step	Equipment type	Why it is needed	Notes from CXMT's published research / typical requirements
Silicon pillar formation	HAR silicon etch	Define the vertical Si pillars (channels)	Needs good verticality and sidewall smoothness. Often ICP or specialised deep Si etch.
Bit-line STI etch (word-line isolation)	Dielectric etch (oxide/SiN) with precise profile control	Etch STI oxide so the sidewall is as vertical as possible	Explicitly called out as critical – tapered etch causes WL-to-WL leakage. Requires tight CD and profile control.
Gate dielectric + TiN gate	ALD (atomic layer deposition)	Conformal thin oxide (often ALD + ISSG) and ALD TiN that fully wrap around the pillar	Essential for true gate-all-around. Thickness and conformality must be very uniform.
Si_3N_4 isolation	CVD / PECVD	Deposit Si_3N_4 to isolate neighbouring word lines	Must fill without voids between closely spaced pillars.
Buried bit line	Ion implanter (medium/high current)	N^+ implant for buried BL + boron implant for isolation	Hot implant in quad mode is used to reduce shadowing and damage. Dose/energy control is important for resistance vs leakage.
Node contact / landing pad	Deposition + etch + CMP	Build the stack between the Si pillar and the capacitor	Needs good planarity and contact resistance control.
Hexagonal capacitor	High-k ALD + electrode deposition + etch	Form the high-k storage capacitor in hexagonal shape	Aspect ratio and uniformity matter for capacitance.
Planarisation	CMP	Flatten after depositions and before subsequent patterning	Multiple CMP steps are typical in this kind of vertical flow.
Contact resistance improvement	Laser anneal or advanced RTA	Reduce contact resistance	Not fully implemented in CXMT's published research but noted as beneficial for drive current.

Source: CXMT, LRCX, UOB Kay Hian

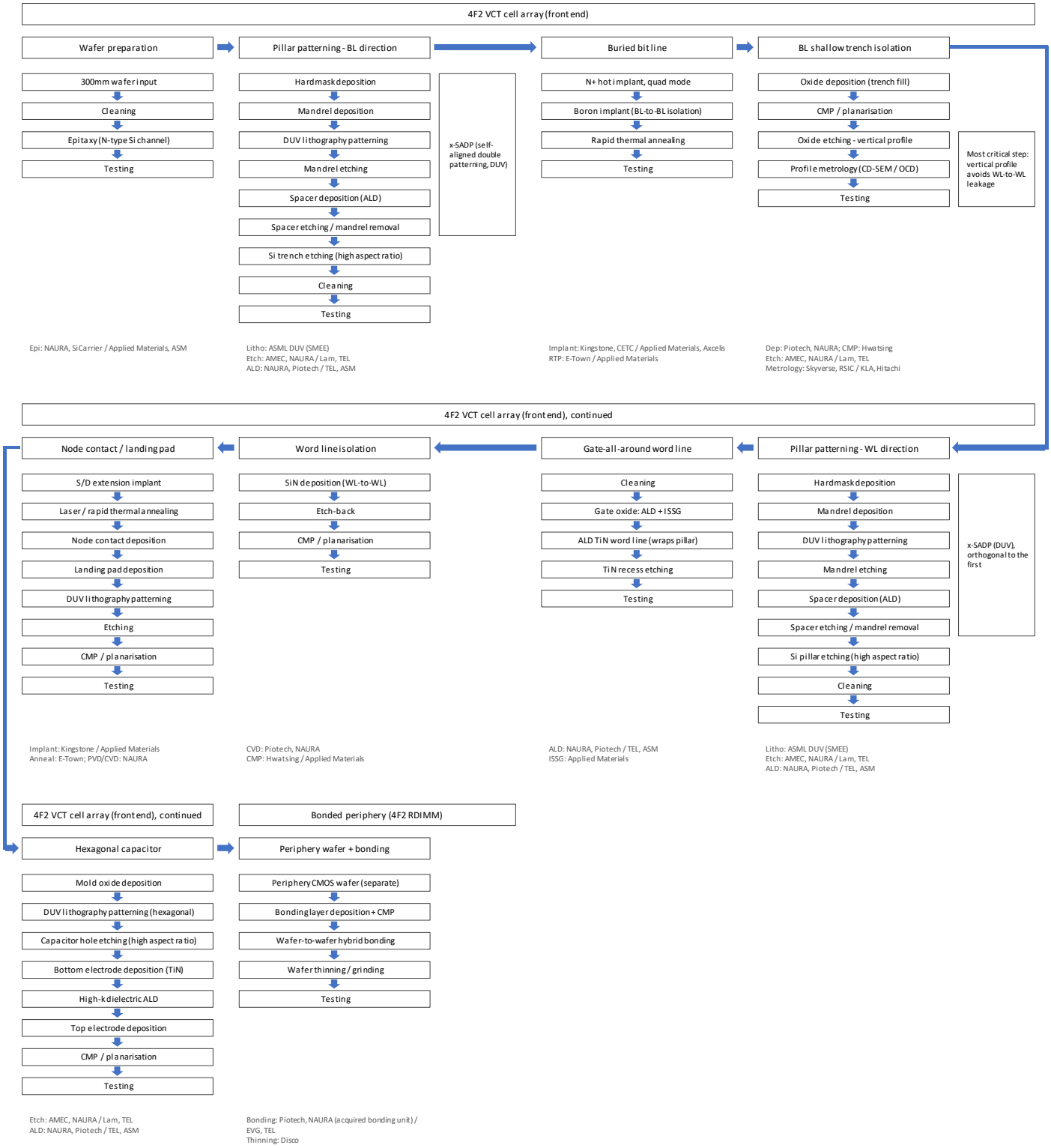
- **We do not believe CXMT can surpass its global peers in technology through the development of next-generation architecture.** Apart from the various downsides of the migration to vertical scaling (ie lower yield, limited access to advanced WFE, lower throughput, and heavy investments), CXMT's vertical scaling is only as good as the quality of its horizontal scaling. It is a fact that CXMT is reaching the ceiling of horizontal scaling without accessing EUVs (or even advanced DUVs), which has forced it to develop vertical scaling technology. As such, a better way to look at next-generation memory architecture is that it provides ways for CXMT to continue catching up with global leaders beyond the technological bottleneck it is facing at the moment.
- For the big 3 global DRAM IDMs, next-generation DRAM architecture is also important, as sub-10nm nodes are increasingly difficult to produce through pure horizontal scaling. However, it is less of a necessity for them than for CXMT/YMTC, and the industry leaders generally have to consider the return on investments, ie how long the technology can last and if the amount of investment is worth it. Thus, major DRAM manufacturers are expected to begin ramping up production of next-generation DRAM technologies later than CXMT. For example, Samsung has indicated that it plans to begin risk production of VCT 4F² DRAM by 2028, while Micron is choosing to skip it entirely and opting to develop 3D DRAM which is now estimated to start seeing adoption beyond 2030-32 at both Micron and Samsung.
- For an outline of the VCT 4F² and 3D DRAM processes and the respective related equipment suppliers, please see the process flow charts on the next page.

Major DRAM IDMs' Stance On Next-generation DRAM Architecture

	SK Hynix	Micron	Samsung	CXMT
Stance	Extend 6F²	6F² only	6F² core; VCT 4F² (D0a-V) in development	Racing to launch 4F²
6F² strategy	Extend via EUV and process scaling	Extend planar 6F² via 1cnm and 1dnm	Continue 1c/1d scaling	G5 in mass production via SAQPm, No EUV
4F² status	Vertical gate DRAM demonstrated in VLSI 2026	Skipping 4F²	16Gb 4F² prototype shown in ISSCC 2026	Server DDR5 RDIMM samples fabbed by 4F² by end-26
Key tech directions	GV+peri-under-cell; 3D DRAM	Directly to 3D DRAM	Vertical transistor (VCT); W2W hybrid bonding	Vertical surround gate transistor (same as VCT)

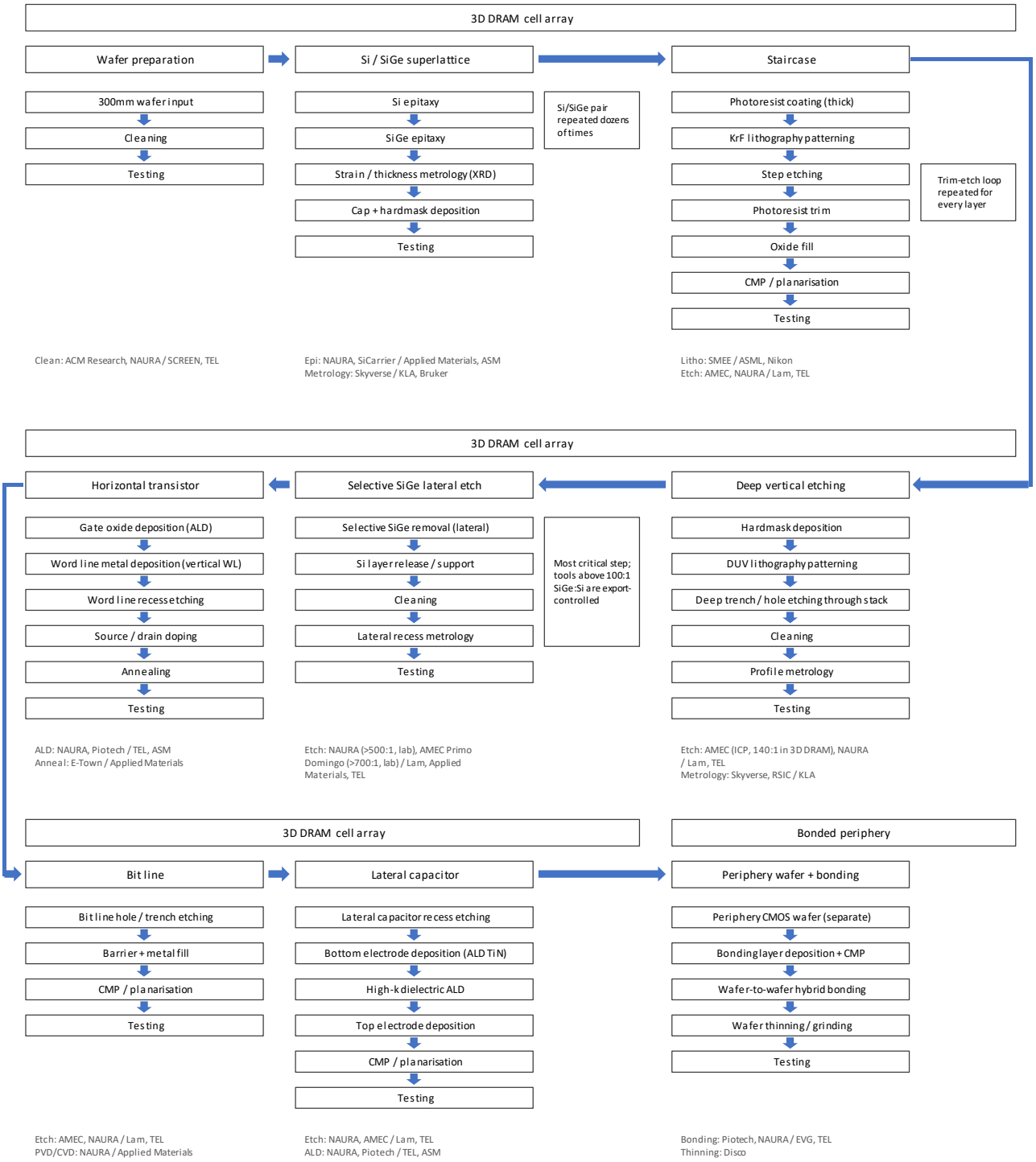
Source: TrendForce, respective companies

Process Flow Of CXMT's DDR5 Server RDIMM Fabricated Through VCT $4F^2$



Source: CXMT, UOB Kay Hian

3D DRAM's Process Differs Greatly From 3D NAND's And Integrates More Steps



Note: There is no 3D DRAM volume production currently, not even at the risk/engineering stage. CXMT has also never disclosed any process steps related to 3D DRAM. Thus, this chart utilises data from the more generic steps of research labs. Actual in-production process steps should have more variations in the future.
Source: CXMT, UOB Kay Hian

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